<<集成电路与系统设计、功率与定时 >

图书基本信息

书名：<<集成电路与系统设计、功率与定时建模、优化与模拟>>

13位ISBN编号：9783540390947

10位ISBN编号：3540390944

出版时间：2006-12

出版时间：湖北辞书出版社

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页数：677

内容概要

This book constitutes the refereed proceedings of the 16th International Workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS 2006, held in Montpellier, France, in September 2006. The 41 revised full papers and 23 revised poster papers presented together with 4 key notes and 3 industrial abstracts were carefully reviewed and selected from numerous submissions. The papers are organized in topical sections on high-level design, power estimation and modeling memory and register files, low-power digital circuits, busses and interconnects, low-power techniques, applications and SoC design, modeling, digital circuits, and reconfigurable and programmable devices.

书籍目录

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