

<<Computer Aided Verif>>

图书基本信息

书名：<<Computer Aided Verification 计算机辅助验证>>

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内容概要

This book constitutes the refereed proceedings of the 18th International Conference on Computer Aided Verification, CAV 2006, held in Seattle, WA, USA in August 2006 as part of the 4th Federated Logic Conference, FLoC 2006. The 35 revised full papers presented together with 10 tool papers and 4 invited papers were carefully reviewed and selected from 144 submissions addressing all current issues in computer aided verification and model checking - from foundational and methodological issues ranging to the evaluation of major tools and systems. The papers are organized in topical sections on automata, arithmetic, SAT and bounded model checking, abstraction/refinement, symbolic trajectory evaluation, property specification and verification, time, concurrency, trees, pushdown systems and boolean programs, termination, abstract interpretation, memory consistency, and shape analysis.

书籍目录

Invited Talks Formal Specifications on Industrial-Strength Code--From Myth to Reality I Think I Voted: E-Voting vs. Democracy Playing with Verification, Planning and Aspects: Unusual Methods for Running Scenario-Based Programs The Ideal of Verified Software

Session 1. Automata Antichains: A New Algorithm for Checking Universality of Finite Automata Safrless Compositional Synthesis. Minimizing Generalized Biichi Automata

Session 2. Tools Papers Ticc: A Tool for Interface Compatibility and Composition FAST Extended Release

Session 3. Arithmetic Don't Care Words with an Application to the Automata-Base Approach for Real Addition A Fast Linear-Arithmetic Solver for DPLL(T)

Session 4. SAT and Bounded Model Checking Bounded Model Checking for Weak Alternating Biichi Automal Deriving Small Unsatisfiable Cores with Dominators

Session 5. Abstraction/Refinement Lazy Abstraction with Interpolants Using Statically Computed Invariants Inside the Predicate Abstraction and Refinement Loop Counterexamples with Loops for Predicate Abstraction

Session 6. Tools Papers Cascade: C Assertion Checker and Deductive Engine YASM: A Software Model-Checker for Verification and Refutati,

Session 7. Symbolic Trajectory Evaluation SAT-Based Assistance in Abstraction Refinement for Symboli, Trajectory Evaluation Automatic Refinement and Vacuity Detection for Symbolic Trajectory Evaluation

Session 8. Property Specification and Verification Session 9. Time Session 10. Tools Papers Session 11. Concurrency

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